

MEDIA ALERT

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Bluespec Showcases Technology Leadership at IP-SOC 2005, VLSI 2006, DesignCon, DVCon

*ESL Synthesis Recognized as Relevant Topic as Technologists, Executives, Customers
Describe Commercial Usage*

Waltham, Mass. — December 13, 2005 — Technologists, executives and customers from Bluespec Inc., developer of the only ESL synthesis toolset for control logic and complex datapaths in chip design, are invited speakers at several technical conferences, including IP-SOC 2005 held this month in Grenoble, France.

This interest in ESL synthesis as a relevant technical topic continues into 2006 with presentations at VLSI 2006, DesignCon 2006 and DVCon 2006. Bluespec Founder Arvind, professor of the Massachusetts Institute of Technology, is the banquet speaker during VLSI 2006 and will discuss, “UNUM: A Tinker-Toy Approach to Building Multicore PowerPC Microarchitectures.”

For more details, contact George Harper, vice president of Bluespec, who can be reached at (781) 250-2200 or via email at george.harper@bluespec.com. Or, visit the Bluespec website located at: <http://www.bluespec.com>.

IP-SOC 2005 (IP-Based SoC Design Conference and Exhibition)

Grenoble, France

Held December 7 -8, 2005

- Paper session titled, “A Case Study in Rule-Based Modeling”
- Presented by: Wolfgang Ecker, Volkan Esen, Thomas Steininger of Infineon Technologies and Mieszko Lis of Bluespec

More information can be found at: <http://www.us.design-reuse.com/ipsoc2005/>

19th International Conference on VLSI Design (VLSI 2006)

Taj Krishna, Hyderabad, India

January 3-7, 2006

- January 3, 9 a.m.: Tutorial Session T3A: Beyond RTL: Advanced Digital System Design
- Presented by: Rishiyur Nikhil and Shiv Tasker of Bluespec
- January 6, 8 p.m: Banquet Speaker: Professor Arvind of the Massachusetts Institute of Technology and Bluespec founder
- Title: “UNUM: An Approach to Building Multicore PowerPC Microarchitectures”

More information can be found at: <http://www.vlsiconference.com/>

DesignCon 2006

Santa Clara Convention Center, Santa Clara, Calif.

February 6-9, 2006

- February 6, 1:30 p.m.: TechForum Tutorial: TF-MP1: Beyond RTL: Advanced Digital System Design
- Description: This tutorial will introduce new technologies and advanced techniques to cope with the complexity of designing modern digital chips which, increasingly, are complete systems containing multiple processors, complex IP blocks and high-speed buses and interconnection networks.
- Presented by: Rishiyur Nikhil of Bluespec
- February 8, 9 a.m.: Management Forum Panel: Make Technical On-Line Marketing Truly “Technical” — From Tactics to Strategy: What Works and What Doesn’t?
- Chairperson: Ed Y. Zhang, Hometown Innovation Automation Inc.
Bluespec panelist: George Harper

More information can be found at: <http://www.designcon.com/2006/index.html>

Design and Verification Conference and Exhibition (DVCon 2006)

Doubletree Hotel, San Jose, Calif.
February 22-24, 2006

- February 23, 11 a.m.: Technical Session 3: A False Dichotomy? High-Level Synthesis and Control: A CPU Case Study
- Presenters: Wolfgang Ecker, Volkan Esen, Thomas Steininger of Infineon Technologies and Mieszko Lis of Bluespec

More information can be found at: <http://www.dvcon.org/>

About Bluespec

Bluespec Inc. manufactures an industry standards-based Electronic Design Automation (EDA) toolset that significantly raises the level of abstraction for hardware design while retaining the ability to automatically synthesize high-quality RTL, without compromising speed, power or area. The toolset, the only one focused on control and complex datapaths, allows ASIC and FPGA designers to reduce design time, bugs and re-spins that contribute to product delays and escalating costs. More information can be found on www.bluespec.com or by calling (781) 250-2200.

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