

NEWS RELEASE

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Bluespec Adds ESL Synthesis to SystemC *Open ESL Synthesis Extensions to SystemC Create Unified Environment for Modeling, Design, Verification*

Waltham, Mass. — May 29, 2006 — Bluespec Inc., developer of the only ESL synthesis toolset for control logic and complex datapaths in chip design, today announced ESL Synthesis support for SystemC, the language that provides hardware-oriented constructs for C++ as a class library.

With this announcement, Bluespec enriches SystemC for hardware architecture and design. It addresses a major issue in the SystemC standard — SystemC-based Electronic System Level (ESL) Synthesis — a unified environment for modeling, design and verification that raises the level of design abstraction above the register transfer level (RTL). In doing so, Bluespec elevates the description and synthesis of control and complex datapaths for SystemC-based designers. It moves SystemC from being just another transaction level modeling (TLM) language with almost no ties to RTL (except algorithmic synthesis) to an accurate modeling language with full hardware architecture and implementation support.

“Until now, SystemC has just been a tantalizing tease for hardware designers,” says Shiv Tasker, chief executive officer of Bluespec. “ESL Synthesis delivers on

SystemC’s promise of a single environment for modeling, design and verification, and is destined to increase its adoption on a broad scale.”

Bluespec’s ESL Synthesis Extensions (ESE, pronounced ēsē) for SystemC add two key enhancements in the areas of concurrency and communications: atomic transactions, or rules; and automated, formal interface contracts, or interface methods. These extensions, as well as the language reference manual (LRM), other documentation and code examples, are freely downloadable and work with the standard OSCI reference simulator, for untimed simulation, and the GNU Compiler Collection (GCC) compiler.

These resources are available on the Bluespec website found at: <http://www.bluespec.com>. Additionally, Bluespec is making the syntax to the extensions open.

ESE simplifies the modeling of complex concurrency over threads and improves model composition through automated, formal interface contracts. Bluespec’s synthesis technology converts ESE designs into efficient RTL.

ESE is meant to be used by SystemC-based architects, hardware designers and verification engineers responsible for a chip’s architecture and modeling. For hardware designers, it offers a higher level of design for control and complex datapaths. Unlike current approaches, it provides a seamless path from architecture exploration to design and verification. It reduces verification cycles and enables the synthesis to RTL code in Verilog with high quality of results (QoR). This Verilog code serves as input to any standard industry flow including RTL synthesis and simulation.

For verification engineers, it simplifies the expression of complex, multiple concurrent activities, while retaining all the other benefits of SystemC for verification. It

accelerates the development of testbenches and offers the option of synthesizing testbenches for rapid prototyping environments.

For architects, ESE provides a single environment for architecture exploration and design implementation, eliminating the need to maintain separate designs between modeling and implementation. It enables more accurate concurrency modeling and introduces the ability to assess the implications of different architectures for power, area, latency and throughput.

Pricing and Availability

Bluespec's ESL Synthesis for SystemC is shipping today and supports Linux operating systems:

- ESE — Free implementation of the ESL Synthesis Extensions to SystemC is available via Bluespec's website. This version supports the ESL Synthesis language extensions for untimed simulations with the standard OSCI SystemC simulator.
- ESEPro — Bluespec's premium implementation of the ESL Synthesis Extensions to SystemC. This version adds support for clock-scheduled simulations enabling both:
 - o Untimed simulations with the standard OSCI SystemC simulator; and,
 - o Clock-Scheduled simulations with the standard OSCI SystemC simulator.

ESEPro pricing starts at \$35,000 for a one year, time-based license.

ESEComp, which synthesizes ESE SystemC designs into Verilog RTL, will be released to customers later this year. All products, including ESEComp, will be demonstrated during the 43rd Design Automation Conference (DAC) July 24-27 at the Moscone Center in San Francisco.

For more details, contact George Harper, Bluespec's vice president of marketing, who can be reached at (781) 250-2200 or via email at info@bluespec.com.

About Bluespec

Bluespec Inc. manufactures an industry standards-based Electronic Design Automation (EDA) toolset that significantly raises the level of abstraction for hardware design while retaining the ability to automatically synthesize high-quality RTL, without compromising speed, power or area. The toolset, the only one focused on control and complex datapaths, allows ASIC and FPGA designers to reduce design time, bugs and re-spins that contribute to product delays and escalating costs. More information can be found on www.bluespec.com or by calling (781) 250-2200.

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