



In this fourth round of **In Play in EDA, Volume 1, Number 4**, Peggy Aycinena speaks with Bluespec, Inc. about sequential versus parallel thinking, and the implications for designing in SystemC versus SystemVerilog. She also glances through the latest textbook on SystemVerilog for design, written by celebrity authors Sutherland, Davidmann, and Flake.

And just in case you missed the other editions this month, you can still read them here:

[In Play in EDA, Volume 1, Number 3](#)

[In Play in EDA, Volume 1, Number 2](#)

[In Play in EDA, Volume 1, Number 1](#)

Celebrities for a New Age

By Peggy Aycinena

Celebrities like Madonna, Cher and Prince share a particular distinction. No one seems to know their last names. In the heady world of academia, however, I can only think of one individual who can lay claim to such a distinction. He's an engineering professor at MIT in Cambridge, Massachusetts, and his name is **Arvind**.

Arvind has been a fixture on the hardware design landscape for a long time. The research attributed to Arvind, or to researchers associated with Arvind, has had a far-ranging impact in many areas. I can't actually prove this, but arguing heuristically, it must be true. Otherwise, why would so many people know him only by this celebrity-like moniker?

But this isn't really the subject at hand. The subject at hand is a recently patented technology that's come out of MIT -- specifically out of Arvind's group -- and an exclusive licensing of that technology, which was announced this week by a MIT-related start-up called [Bluespec, Inc.](#)

Bluespec says it has developed the industry's first high-level SystemVerilog-based EDA toolset and that MIT has granted the company a license for its "groundbreaking" Term Rewriting System [TRS] based synthesis technology to be used as a foundation for

the company's EDA toolset.

To put it in Bluespec's words: "TRS is a computational model that enables high-level hardware synthesis with results, for the first time, that match hand-coded RTL, fundamentally changing the way engineers can approach hardware generation. TRS alters the approach to ASIC/FPGA creation by attacking root design issues."

That sounded pretty groundbreaking to me -- especially because Bluespec has "wrapped the TRS model with SystemVerilog" -- and that statement prompted a phone conversation with **Rishiyur Nikhil**, CTO at Bluespec. One can never hear too much about SystemVerilog, particularly in the emerging "Age of SystemC."

Nikhil told me, "I was on the faculty at MIT until 1991. While I was there, I worked closely with Arvind. In fact, we have dozens of joint publications and a textbook that we wrote -- it's been a very close collaboration. Even after I left MIT, I worked at the Cambridge Research Lab, where we continued our collaboration through the 1990's."

"Bluespec, the company, originated in research in Arvind's group. Arvind and I are the co-founders of Bluespec and he is still a member of our board. The research that Arvind's group continues to do at MIT is very closely tied up with what we do at Bluespec. There's a lot of joint work going on between his grad students and our company and, in fact, we're expecting to hire some people out of his group."

As interesting as those details about Bluespec were, what I really wanted Nikhil to talk about was SystemVerilog versus SystemC. He was more than willing: "Let me start by contrasting C and SystemC approaches with SystemVerilog. The goal in both cases is to get to higher levels of abstraction."

"Generally, when people go to a higher level -- a behavioral description or an algorithmic description -- all of the terms used indicate a desire to express the design in traditional software terms. Synopsys had Behavioral Compiler, for instance, which was going in the same direction, but they're no longer supporting it. There's a reason for that and a common theme here."

"At the behavioral, algorithmic, or high level of design, code-functionality notation is similar to a sequential language like C, and design efforts revolve around automatically producing hardware from those descriptions. Arvind and I are not very enthusiastic about that approach, however."

"There's been a long history in the design community of trying to take sequential notation like C or FORTRAN and use it for hardware design. In fact, between the two of us, Arvind and I have spent 40 or 50 years looking at these things and we know the approaches

have not really panned out. We have strong credentials in this area and we believe, after researching the whole process of getting from sequential to parallel, that we can hold our own in any argument against sequential design strategies."

"The principle problem is with the model in which you are thinking as a designer when you're coding at the level. That model is very, very different from how you think in hardware. In C, it's a sequential process, one with recursion stacks, for instance, and conventional models of execution."

"It's true that a very complex function can be easily written in C, but that code says absolutely nothing about what kind of architecture you may want. Do you want a pipeline architecture, what different kind of look-up algorithms do you want, and so forth? We feel that there's just too big of a gap between the way a designer tends to think in C and how a designer thinks in hardware."

"C is a completely sequential language so it's not a good language for expressing the parallelism found in hardware. Because it's not feasible to go from sequential notation to parallel notation, we're very skeptical that C will work for hardware design."

"Now it's true -- SystemC is slightly different. It includes some notation explicitly designed for parallel notation, but it's still very much a software model. In fact, whenever we talk to engineers, they tell us they feel like they're wading away from the shore when they work in SystemC. Pretty soon they feel like their feet don't hit the ground. And this is not just a feeling -- it's a very hard technical problem to go from that notation to hardware."

"At Bluespec, at a certain level, our tool is very similar to what engineers are already doing in Verilog or SystemVerilog. They choose a model for their system circuit -- the architectural parameters of that circuit -- and all of it is written explicitly in SystemVerilog. Designers absolutely want control at a level similar to sketching the thing out on a white board and we stay with that in the Bluespec tool."

"Where Bluespec improves on SystemVerilog, however, is in how you improve the system architecture. We provide rules or design assertions -- you can think of the rule as describing one aspect of the behavior of the circuit. A rule captures both a state change and the conditions under which it can occur. The MIT technology makes it possible to generate efficient hardware from a TRS-based design. It generates optimized circuitry for scheduling the rules, allowing many to fire simultaneously, while remaining faithful to the one-at-a semantics of TRS."

"There is a processor analogy here. You may be processing an instruction, perhaps an add instruction, and typically you have one

rule to do that: read some value, do an add operation, store the results. There are analogous rules for branch calls, etc. You can describe the full behavior of your processor with a set of rules, and those rules look very much like what you would find in the instruction manual for the processor"

"What the Bluespec compiler does is to analyze all of those rules, and produce hardware for those rules including the hardware that allows the rules to work concurrently. In a modern processor, for example, if you have a memory load and an add instruction, those can be done in parallel unless the value produced by one instruction feeds into the other. Our compiler will automatically determine where it is safe for instructions to go in parallel. In places where they feed into one another, our compiler will provide for that as well. The result is a very powerful tool that can deal with concurrency. The designer now has a complete and intuitive level of control over concurrency -- even over race conditions, which is always a big problem."

"In other words, to get back to the story of C versus SystemVerilog; at Bluespec we stay with the model that hardware designers need to think about finite state machines working in cooperation with each other. We've automated that model, but we have not moved to the less advantageous software model. We feel very comfortable with our ability to provide high quality RTL using our tool."

"And, returning to the software analogy, one more time -- in software, we've moved from Assembly to C, C++, and now Java. All of these languages are, theoretically, equivalent. Anything that can be expressed in one language can be done in another language. But, it's far easier in Java, specifically because we can express things in abstraction rather than getting into the busy work and minute details of coding in Assembly. We're trying to do that exact same thing here at Bluespec. Historically, the move was from schematic capture up to RTL, and then to SystemVerilog. Now, we're providing the next step."

As Nikhil wrapped up, he outlined Bluespec's involvement with Accellera: "Accellera runs SystemVerilog, and there are four technical committees associated with that effort. There is one committee aimed at the designers, and we have been an active participant in that committee, reviewing many of the chapters of the upcoming SystemVerilog manual. As a company, we've donated many of the ideas in use there. Our ideas have been voted on and accepted, and are now part of the third draft."

I thanked Nikhil for the discussion and we closed out our phone call. As I turned back to the pile on my desk, I was struck by the coincidence of receiving in that day's mail a copy of the new Kluwer Press title, "SystemVerilog for Design," written by **Stu Sutherland**, **Simon Davidmann**, and **Peter Flake**. Certainly, if there ever were celebrities in the SystemVerilog world, these guys are among them.

Included in their ranks, of course, would also be **Phil Moorby**.

I thumbed through the book and it was obvious to anybody interested in SystemVerilog, that this is a must read. The book is lengthy, detailed, and well laid out. But the best part is in the Appendix.

If you're interested in celebrity as well as SystemVerilog, that's where you'll find photos of the whole pantheon of stars involved in the development of the language- - photos going back 20 years, from 1981 to 2002. Those photos, in combination with the notes and historical comments, are most definitely worth the price of admission. In fact, maybe, like entertainers and rock stars, they could take the whole thing on the road. Surely tickets to "SystemVerilog: The Reunion Tour" would sell like hot cakes -- even if the players in the band do have two names apiece.

EDA Players

The [EDA Consortium's \(EDAC's\) Market Statistics Service \(MSS\)](#) announced that EDA industry revenue for Q4 2003 was \$1.021 billion, a 13-percent increase over Q4 2002. MSS said this is the first time in two years that industry revenue topped \$1 billion, and the first quarter since Q1 2001 that the industry has had double-digit revenue growth. Total 2003 revenue was reported to be \$3.825 billion, an increase of 3 percent over 2002. In addition, MSS reported Q4 2003 employment in EDA companies rose 4 percent over Q4 2002, to a total of 18,900.

EDAC Chairman and Mentor Graphics CEO, **Wally Rhines**, is quoted: "In the fourth quarter of 2003 the EDA industry showed a return to solid growth. It appears that the strength of recovery in the semiconductor and systems industries is having a good effect on EDA."

[AccelChip Inc.](#) announced that it has signed Parallel Systems Ltd. to distribute its products, IP, and services in the U.K. and Ireland. [Emulation and Verification Engineering \(EVE\)](#) announced it is now an official EDA Partner of [ARM](#). The companies say that membership in the Partner Program will enable EVE's products to support ARM core-based developers. Additionally, EVE has joined the ARM RealView Model Library (RVML) Access Program, and that Model Library components have been integrated with EVE's hardware-assisted verification platform.

The **International Society for Quality Electronic Design (ISQED)** announced that **Synopsys** President and COO **Chi-Foon Chan** has been named at the first ISQED fellow at the ISQED04 conference in San Jose. Chan has been with Synopsys since 1990, and is currently also a member of the company's Board of Directors. Previously, Chan was with NEC Corp. and Intel Corp. He has an M.S. and Ph.D. in Computer Engineering from Case Western

Reserve University. ISQED Chairman, **Ali Iranmanesh**, is quoted: "Dr. Chan has played a crucial role in steering the ISQED symposium since its initiation in 2000. His expertise and understanding of both design-for-manufacturing and IC quality have been critical in establishing us as a world-class technical forum. His continued support and direction clearly merit this fellowship."

[OEA International, Inc. \(OEA\)](#) has joined the Synopsys in-Sync program. The companies say the move will improve interoperability between Synopsys' HSPICE and OEA's NET-AN's 3D interconnect parasitic extraction tool. HSPICE will be used to verify SPICE sub-circuit models produced by OEA software to assure correct operations of the flows of mutual customers.

[SAME 2004](#) - The seventh annual conference and tutorials will be addressing state-of-the-art developments in the design and manufacturing of ICs and systems in Sophia Antipolis, France, on October 6th and 7th. Topics will include mixed-signal and RF design; design tools and methodologies; system architecture and embedded systems; power management; micro packaging and SIP (system-in-package) design. The May 2nd deadline for paper submission is fast approaching.

[Synopsys, Inc.](#) announced the opening of an expanded Shanghai office, complete with R&D center and office space for 200+ sales, R&D, and technical support staff. Company President and COO Chi-Foon Chan was at the ribbon-cutting ceremony, as was company executives Yu Zhong-Yu, member of National Committee of the CPPCC and President of China Semiconductor Industry Association; Feng Ji Chun, Director of Department of High and New Technology and Industrialization, Ministry of Science and Technology P.R.C (MOST); key clients and strategic partners.

Yu Zhong-Yu of the CPPCC and China Semiconductor Industry Association is quoted: "China's semiconductor industry has maintained strong development momentum in recent years. First, technological advancement has accelerated and breakthroughs have been achieved in semiconductor design, manufacturing, packaging, and testing. Second, a favorable cycle has been established for capital investment. Close cooperation with international companies has played a key role in promoting the development of China's semiconductor industry. By increasing its focus on the China market, we believe Synopsys, the world leading company in the electronic design automation industry, will become a valuable long-term player in China's semiconductor industry."

The Play Book

[Virage Logic Corp.](#) announced that Virage Logic's Technology-Optimized Platform and its Area, Speed and Power (ASAP) Logic Metal Programmable Cell Libraries are now available on the jointly developed **Chartered Semiconductor Manufacturing** and **IBM**

90-nanometer manufacturing process. The companies say that SoC designers now have access to Virage Logic's IP as part of the semiconductor industry's "first common cross-foundry design enablement program starting at 90 nanometers, announced separately by IBM and Chartered."

[True Circuits, Inc. \(TCI\)](#) announced that **Ubicom, Inc.** has implemented multiple TCI PLL hard macros in Ubicom's IP3023 wireless network processor using TSMC's 130-nanometer process technology. The companies say that the Ubicom processor is now in volume production. [Synopsys, Inc.](#) announced that **Motorola Inc.'s Semiconductor Products Sector (SPS)** has expanded its agreement to license Synopsys' phase-shift technology and mask synthesis software for its 90-nanometer SOI (silicon-on-insulator) process technology.

Also from Synopsys: The company, in conjunction with [Jungo Software Technologies, Inc.](#), announced that the companies are partnering to offer a hardware and software USB full speed On-The-Go (FS-OTG) package, which includes Synopsys DesignWare IP and Jungo software. Together, Jungo and Synopsys reported that the OTG hardware and software work in tandem to perform all FS-OTG functions. Jungo says it used the FPGA-based DesignWare FS-OTG hardware development platform to create specific driver software to match Synopsys' USB FS-OTG core.

[Nassda Corp.](#) announced that **Sirific Wireless Corp.** has adopted Nassda's HSIM full-chip simulation and analysis tool for top-level verification of its GHz-frequency wireless semiconductor designs. The companies report that Sirific engineers used HSIM to complete detailed timing and power analysis on a 60K-transistor design in 3.3 hours. Then they took a break for lunch.

[MIPS Technologies, Inc.](#) and **Green Hills Software, Inc.** announced that Green Hills's software development tools for MIPS-Based applications supports the new MIPS32 24K core family. The tool set has been optimized for the MIPS32 and MIPS64 architectures, and integrates the Green Hills MULTI IDE with simulators from MIPS, a hardware debug probe, and OS support across a range of applications.

[Mentor Graphics Corp.](#) announced the release of its Capital Analysis tool suite, which is an addition to the Capital Harness Systems (CHS) data-centric end-to-end toolset for complex wiring systems design, analysis, and manufacture. Capital Analysis is available as part of Release 3 of Capital Harness Systems, and is designed for the analysis of electrical wiring systems design in the automotive, rail and aerospace industries. Capital Analysis is used to validate design intent early in the design process with electrical simulation, sneak circuit and failure mode effects analysis (FMEA) tools. It also provides automated FMEA reports. The initial release includes twelve products for logical and DC simulation, automated

FMEA report generation, sneak-circuit and stress-analysis, scripted simulation and support for back-end service documentation production.

[Manhattan Routing Inc.](#) announced that [ChipWrights Inc.](#) used Manhattan's Physical Window design visualization environment to meet timing specifications for an 0.18-micron image processing DSP, a 200MHz ASIC design with 1.5 million logic gates. Director of Engineering at ChipWrights, **Mike Goldman**, is quoted: "Physical Window gave us tremendous bang for the buck. It was a cost-effective method for communicating with our vendor's physical implementation team. Without Physical Window, we would have had to either be on-site at the vendor every time we needed to view the layout, or else purchase expensive layout tools to do it in-house."

[Magma Design Automation](#)'s Silicon Correlation Division announced that **Mindspeed Technologies, Inc.** has standardized on Magma's SiliconSmart CR for timing and power characterization of their nanometer libraries. Mindspeed says their decision was based on an evaluation of the product and the success of SiliconSmart CR at Conexant Systems, Inc., the former parent company of Mindspeed.

[LogicVision, Inc.](#) is branching out. The company has announced the formation of a new service organization, D2X Solutions, which will offer design-to-manufacturing services and IC supply chain management consultation to OEMs, IDMs, and system houses. Services will include program management and technical support services that can be applied throughout the supply chain, including flexible design service engagement models for RTL-to-tapeout chip design, silicon debug, production test of ICs, board and system level test, and field service.

The company says that D2X will provide technical process analysis to companies as well as specific recommendations for meeting high-level economic goals -- increased yield, higher product quality, cost savings, and faster time-to-volume. LogicVision is currently working with selected IDM customers and system houses and plans to extend its consultation and service offerings to other customers in the immediate future.

[HARDI Electronics AB](#) announced the availability of a new daughter board that permits PCI/PCI-X connectivity to the company's HAPS prototyping system. The new PCIX board serves as a platform for verifying PCI-X cores and as a direct connection between a HAPS system and a PCI/PCI-X bus. Designers can either place the PCIX board in a PCI (or PCI-X) slot in a computer or stack it directly on a HAPS motherboard.

[DFM](#) announced it supports the Cadence Allegro system interconnect design platform. The company's MakeDO technology works with the Allegro platform for routing high-speed constrained

designs.

[Actel Corp.](#) announced it has received the ISO 9001:2000 certificate by the Defense Supply Center of Columbus (DSCC). The company also announced that its antifuse-based FPGAs have received a QML 38535 certificate, which the company says assures compliance by Actel's products with the quality and reliability standards required for use in military and space applications.

Editor's Note - Take a moment to review the various standards acronyms here:

ISO - International Organization for Standardization

QML - Qualified Manufacturers List - a list of those who holds a PRI certificate for being in compliance with AS7003 and/or portions of AS9000

PRI - Performance Review Institute, an affiliate of SAE

SAE - Society of Automotive Engineers

AS9000 - Aerospace Quality Assurance

AS7003 - National Aerospace and Defense Contractors Accreditation Program

Also from Actel Corp.: The company has introduced a third element in its MIL-STD-1553 portfolio, the Core1553BRM IP core, which is designed for use with Actel's FPGAs. The software-programmable Core1553BRM allows designers to select an integrated, individual or dual-function bus-controller, remote-terminal, or monitor-terminal solution. The core is both MIL-STD-1553A and MIL-STD-1553B compliant and is described by the company as reducing system costs in comparison with custom ASIC solutions.

[Aldec, Inc.](#) announced that the company's tools have been selected as the "recommended verification solution" at the Shanghai IC Center (Shanghai ICC) in China. Says Aldec: "With the Shanghai ICC's selection of Aldec, all FPGA-based design training for emerging companies in the region will be based on Aldec tools. The Shanghai ICC is located in the one of the fastest-growing semiconductor regions in the world. Supported by the Chinese Ministry of Science and Technology, Shanghai ICC is the leading organization among the seven National IC Bases. The IC bases provide Chinese companies with access to leading EDA tools for both front-end and back-end design. China's design centers have brought the country to an advanced level of electronics design."

A recent joint study by **Gartner Dataquest** stated that China will soon challenge other Asia-Pacific countries for the number one position in terms of EDA market size. Most recent data shows that China accounted for almost 1.5 percent of the worldwide software revenue for EDA, and this is expected to grow at a five-year compound annual growth rate (CAGR) of about 25 percent in 2006."

The Halftime Program: Peace in our time

Every time I turn around, I'm receiving a press release announcing yet another partnership between an EDA enterprise and one or more governmental agencies in the People's Republic of China (PRC). The chip industry is growing at a staggering rate in the PRC, and naturally the EDA industry wants its share of the spoils.

Yet, current news reports predict that within a handful of years, China's technology will have advanced to a point where their nuclear weapons and delivery systems will be capable of making house calls in Europe, Japan, or North America -- not that they would, of course, but they could if they wanted to, eventually.

Developing weapons systems requires on a lot of state-of-the-art technology, and that technology needs solid tools to advance. Of course, developing new consumer products also requires a lot of state-of-the-art technology and tools. Either way, we all know that where there's a need for tools, there's a potential market for EDA.

Is the PRC then just an enormous market opportunity -- the most promising one in the world today -- or is it, at the same time, an enormous potential enemy? Should it matter to China's trading partners that the market constraints, employment practices, intellectual property protection, and political infrastructures in this emerging giant are problematic at best? Are the contentious and highly charged issues between Taiwan and China of any concern to the rest of us? Do members of the EDA community have any obligation to consider these matters as they aggressively pursue new users in the most populous country on earth?

Clearly, I don't have the answers to these questions and certainly none of it is easy to sort out. But I do think it's appropriate to engage in a dialog about these issues -- a dialog that, in my opinion, is simply not happening within the EDA community. I have yet to hear a single senior executive in EDA honestly and openly address these concerns in public, or do anything more than offer the usual platitudes:

"We have an obligation to our investors and share holders to pursue all possible markets."

"If we don't sell into that market, our competition will."

"The best way to promote freedom and modernism in emerging markets is to engage those markets in mutually beneficial commerce."

"We only sell them the tools -- we're not responsible for what they do with them once they've got them."

If these are just platitudes, what would I prefer to hear from the leadership in EDA?

For starters, I'd like to hear the leadership acknowledge that they're as concerned about these matters as many of the rest of us are. Second, I'd like to hear them acknowledge that the decisions that they're making today might have unforeseen consequences tomorrow -- and admit that they're as unsure about those consequences as those of us less-visionary mortals. Finally, and most of all, for once I'd like to hear them step down from their scripted pedestals and speak about the situation as if we're all in this together. Because we are.

Peggy Aycinena is a Contributing Editor at SOCcentral and can be reached at peggy@soccentral.com



**1st International
System-on-Chip
Conference
April 19 & 20, 2004
Radisson Hotel
Newport Beach,
California**

The **1st International System-on-Chip Conference** is a must for design engineers, technical and marketing professionals, system architects, system platforms designers, executives and business decision-makers in technology companies, engineering professors and students. In short, anyone who needs the latest information on SoC-related technologies, configurable CPUs and DSPs for SoC design, 90nm and sub-90nm challenges, EDA tools for nanometer SoCs, SoC platform design, and suppliers of Intellectual Property.

**[Program Summary](#)
[Program Details and Presenters' Bios](#)**

To unsubscribe to this newsletter, simply email a reply to [Newsletter Administrator](#) with the Subject "Unsubscribe."
You'll be removed from the mailing list immediately.
This newsletter is published by Tech Pro Communications, P.O. Box 1801, Merrimack, NH 03054 603-429-3003