

A high-level alternative to writing RTL, Bluespec is reinventing hardware design for ASICs and FPGAs with the only ESL synthesis solutions that address control logic, complex datapaths and algorithms. Bluespec's ESL is fully synthesizable without compromise in area, speed or latency. The Bluespec toolset allows ASIC and FPGA designers to dramatically reduce design time, bugs, verification resources and re-spins that contribute to product delays and escalating costs. Product highlights:

- Significantly raises the level of abstraction with executable specifications for faster time to completed designs
- Seamless integration with current tools and methodologies, including support for multiple clock domains and verification assertions
- Utilizes HW-centric design language based on industry standard SystemVerilog and Verilog, familiar to engineers
- Maintains the designer's intent - Bluespec makes the designer faster and more accurate by delivering a better design. Bluespec does not try to think for the designer by inventing architecture.
- Synthesizes control logic for correct-by-compiler construction, while retaining 100% of the designer's structure and intent
- Generates no compromise Verilog HW & cycle-accurate models

Tremendous attention has been placed on the mounting cost and schedule issues of verification and timing closure. This focus has overlooked the root cause problem - spiraling design complexities. Verilog and VHDL have changed little in over fifteen years. Designers are stuck trying to construct multi-million gate designs at too low a level, with outdated tools. Low level design composition is contributing to the downstream verification problem by causing more bugs and making the timing closure problem more acute by limiting designer options.

Bluespec attacks the source of the problem, making the ASIC or FPGA designer's job faster and more accurate. By accelerating and improving the quality of designs, Bluespec greatly improves the verification, both with a faster schedule and fewer resources. And by designing in an environment where the micro-architecture can be safely changed, Bluespec designers can confidently effect timing closure instead of trying to close timing sub-optimally by avoiding risky, late stage RTL changes.

Benefits to the Designer

Bluespec enables designers to:

- Accelerate time to verified design by at least 50%
- Reduce both bugs and verification costs by more than 50%
- Retain flexibility to make rapid changes late in the design cycle
- Experience unparalleled reuse, including faster derivatives
- Enable rapid timing closure
- Leverage a unified environment for transaction level modeling through to hardware generation
- Deliver safe, low-impact ECOs that do not disrupt designs

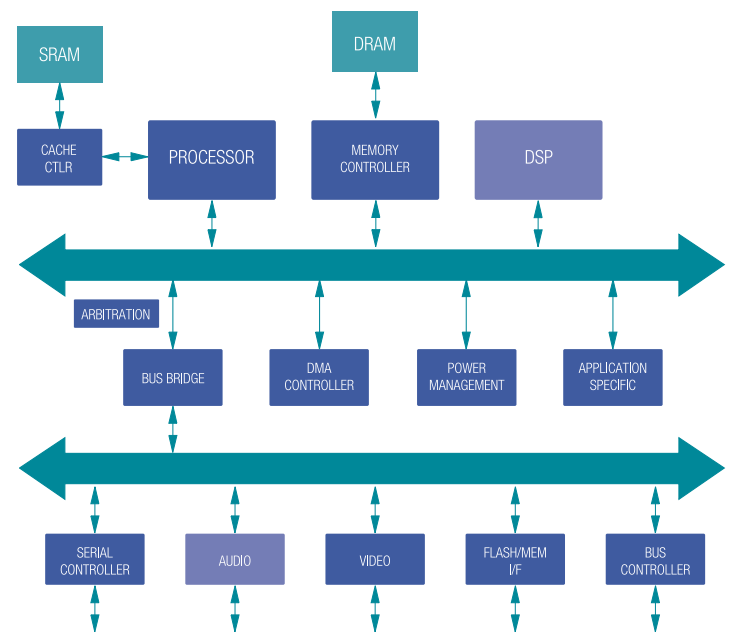
Raising the Level of Abstraction

There have been multiple attempts at attacking design complexity, the root cause behind many ASIC and FPGA development issues. While all have raised the level of abstraction in some way, they have been unable to deliver both modeling abstraction and hardware generation rivaling hand design.

Attempts have fallen into two camps. First, behavioral synthesis takes hardware described very abstractly, often using software constructs, and proposes both architectures and implementations. While a seductive concept, the reality has inevitably been inferior hardware, in area and speed. As attractive the notion that computers can determine optimal architectural and implementation approaches from an abstract algorithm, the problems are far too complex and the solution spaces too expansive.

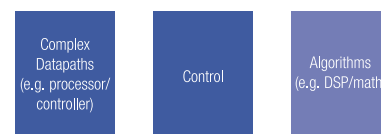
The second approach has been with C/C++/SystemC. As C provides a higher layer of abstraction and is already used as a modeling language by some, it has been tempting to exploit it for hardware implementation as well. Fundamentally, this requires technology that can translate sequential software semantics into parallel, state machine-based hardware. But, there is a problem - this capability has proven to have success in certain limited scenarios (e.g., loop-and-array computations as found in many DSP algorithms),

Bluespec™ ESL Synthesis



DESIGNS COMPLETED WITH BLUESPEC

RISC Processor MIPS IA-64 Power Processor L2 Cache Ctr DDR2 Ctr PCI Express	SRAM Ctr Bus Converters AMBA DMA Ctr Network Processors USB (PHY) PCI-X 802.11a	Queuing Engines Sorting Queue Arbiter IP Lookup Debug Controller OCP Interconnect Ethernet MAC	I2C Pixel Processor Waveform Generator Pong AES	H.264 MPEG-4 IDCT Motion Compensator DES IFFT FIR Filter
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Bluespec is the only ESL synthesis solution that also addresses control and complex datapaths.

in several decades of research in parallelizing compilers. Despite tremendous investments, the semantic chasm between sequential software models and parallel hardware models has proven to be too wide.

Bluespec Approach

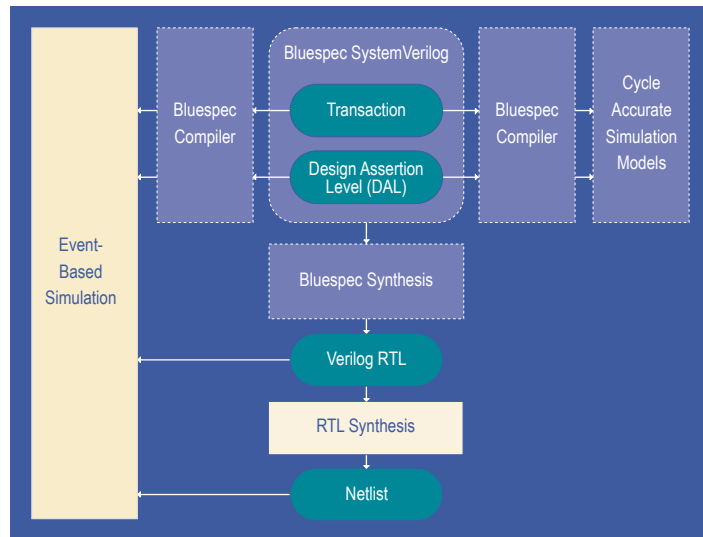
In contrast to previous approaches, Bluespec raises the level of abstraction without compromising the quality of hardware generated. Using familiar hardware semantics, Bluespec builds on RTL by leveraging the same hardware intuitions, providing the designer transparency, predictability and control over the architecture and micro-architecture, and integrating with the same Verilog and VHDL toolsets and flows already in place. On this strong, hardware centric foundation, Bluespec adds a powerful new way to express concurrency and inter-module communications, not available in any other Hardware Design Language (HDL) or modeling language:

- High-level description of behavior (Rules and Interface Methods) resulting in designs that are more succinct, more correct-by-construction, and easier to verify
- Very powerful interface semantics, which enhance correctness when an IP block is plugged into varying environments and automatically manage resource sharing
- Very high degree of parameterization, which greatly improves reuse
- Strong support for embedded assertions, multiple clock domains and gated clocks

Bluespec has been successfully used in designs as diverse as (partial list):

- Controllers: memory/cache/DMA/serial/peripheral
- Bus Interfaces/Converters/Arbiters
- Network Processors
- PHYs
- Queuing/Sorting Engines
- Processors, RISC and CISC
- Pixel Processors
- H.264
- 802.11
- Ethernet MAC

Designers have the option of writing their designs at different levels, from transaction-level to implementation-targeted hardware. When starting intentionally high, designers can perform, at their control, a series of successive refinement steps on the design.



Different parts of the design can be at different levels and progressively they become closer to the hardware - all in the same environment and all with the same design. For the first time, Bluespec offers a unified design environment where designs can be architected, modeled, rapidly prototyped, and hardware generated that competes with hand-crafted designs.

Design Flow

As illustrated by the design flow diagram (below left), Bluespec is designed to fit into current, Verilog-based tools without interrupting your current flow. Bluespec produces either:

- Verilog, for use with current Verilog synthesis and accelerated simulation tools (or)
- Cycle accurate execution models, for accelerated simulation at the source-level

Additionally, Bluespec is completely interoperable with Verilog based designs. Bluespec can easily incorporate Verilog IP - alternatively, Bluespec can be used within Verilog implementations.

Bluespec sits directly in front of current design flows. The designer specifies the design using Bluespec SystemVerilog and generates Verilog output or cycle accurate execution models.

Tool Capabilities

As the first effective ESL synthesis compiler and simulator, Bluespec's toolset provides a unique mix of capabilities. The Bluespec toolset includes both the Compiler and Simulator.

Bluespec Compiler (BSC)

Key features:

- Bluespec SystemVerilog with rules and interface methods
- Generation of no compromise Verilog RTL
- Correct-by-compiler construction of control and datapath logic
- Comprehensive static verification of designs to eliminate problems before simulation
- Code succinctness and static elaboration for high-level abstractness, up to 15:1 code compression, and code reuse
- Integrates into and with existing Verilog/VHDL/SystemC IP
- Rich library of design building blocks
- Integrated compiler algorithms and techniques:
 - Automated and user-defined scheduling of hardware
 - Scheduling visualization and feedback
 - Resource assignment, optimization
 - Standard optimizations, including common sub-expression elimination and logic

Bluespec Simulator (Bluesim)

Key features:

- Accelerated source-level simulation of the high-level design
- 100% cycle accurate with Verilog RTL
- Generates standard VCD files
- 3X-10X faster than traditional event-based simulators

Both BSC and Bluesim were designed for and tested with Linux Red Hat 9.0, Enterprise 3.0 or equivalent.

Unique Core Technology: Term Rewriting Systems

Bluespec's patented technology is based on over seven years of commercial development and nine years of research at MIT. At the core of Bluespec's compiler technology is the introduction of the application of Term Rewriting Systems (TRS) to hardware synthesis. Term Rewriting Systems are a well-understood formalism from computer science. A TRS consists of "terms" which describe hardware states, and "rules" which describe behavior. A "rule" captures both a state change (an "action") and the conditions under which it can occur. As the rules in a Term Rewriting System have atomic semantics, analysis of hardware can be done even though it may be highly concurrent and complex. Commercial projects based on this technology have shown a reduction in DV time ranging from 50% to 70% immediately following initial training.

Further information can be read on www.bluespec.com about additional technical solution areas such as verification time reduction and low power optimization.

Bluespec's three day training course gives designers the tools they need to be successful and show material productivity improvement on their first project. Please contact your sales representative to sign up.